Table of Contents:

List of figures:

Oscillograms:

1. INTRODUCTION.

In this report a description is given of a mains isolated flyback convertor and evaluation board for economy TV. The SMPS has been designed for a maximum average output power of 55W and operates at a mains input voltage range of 90-265Vrms, 50-60Hz.
No opto-coupler is required, because the feedback for the power supply is taken from the non-isolated side of the SMPS transformer.
The key components of the SMPS are the control IC TDA8380, the foil wound SMPS transformer AT3010/110LL and the BUT11A power switching transistor. The output voltages are: 115V, 26V and 16V.

To limit the output voltages and to reduce the input power of the SMPS, special attention has been paid to the standby mode. In this mode the power supply is still operational and can supply the remote circuits. Moreover the SMPS still operates in the fixed frequency mode so no annoying noise will be heard. For testing purposes no pre-load is required.
A printed circuit board (PR35534) has been designed incorporating the 55W SMPS with mainsfilter.

In Chapter 7 and 12-14 information is given concerning a mains isolated 55W SMPS for 220Vrms only, incorporating the TDA8380 control IC, the foil wound SMPS transformer AT3010/90L and the power switching transistor BUT11A. This power supply is also intended for economy TV.
A printed circuit board (PR35552) has been designed incorporating the 55W SMPS with mainsfilter.

On pages 21 and 22 the circuit diagrams are given of two Switched Mode Power Supplies, equipped with a Power MOSFET.

2. CIRCUIT DESCRIPTION.

2.1 Blockdiagram.

Figure 1 shows the block diagram of the 55W flyback converter, with feedback from the "hot" side, which is intended for a mains voltage range of 90-265Vrms.

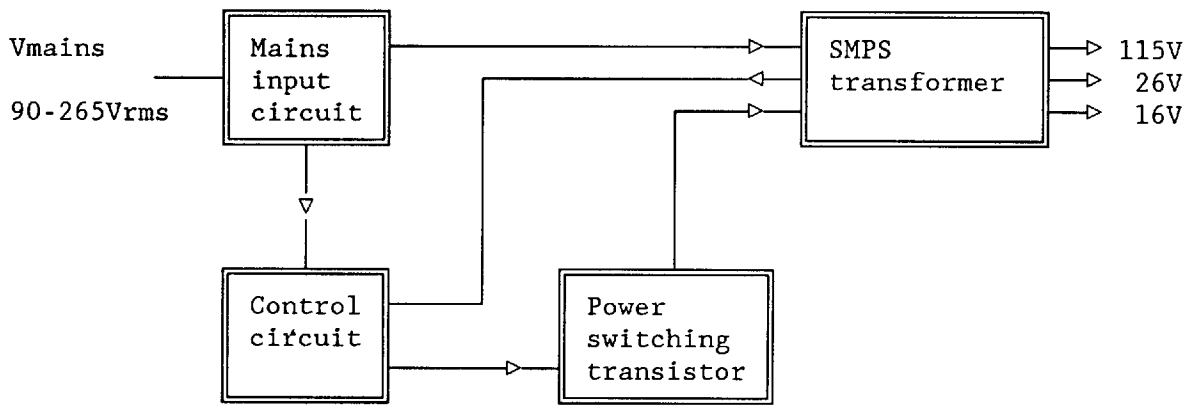

Figure 1: Block diagram

The 55W SMPS evaluation board contains an RFI filter, a fuse and degaussing circuit. The mains input voltage is rectified by bridge rectifying diodes and the DC voltage for the SMPS transformer (AT3010/110LL) is smoothed by a buffer capacitor.

The control IC (TDA8380) derives its start-up supply from this DC voltage and as soon as the IC supply voltage exceeds a certain limit, the IC is initialised. Hereafter the duty factor of the SMPS power switching transistor (BUT11A) increases slowly and its rate of increase is controlled until the SMPS output voltage reaches its nominal level. The take-over supply is derived from a flyback rectifier, which is connected to an auxiliary winding of the SMPS transformer.

The SMPS is a flyback converter, operating on a fixed frequency in the interrupting current mode. At the mains isolated side three flyback voltages are rectified. At the non-isolated side a flyback voltage is rectified and fed back via an attenuator circuit to the error amplifier in the TDA8380. In the standby mode the output voltages remain present.

2.2 Basic operation.

Figure 2 shows the basic circuit of the mains isolated flyback converter.

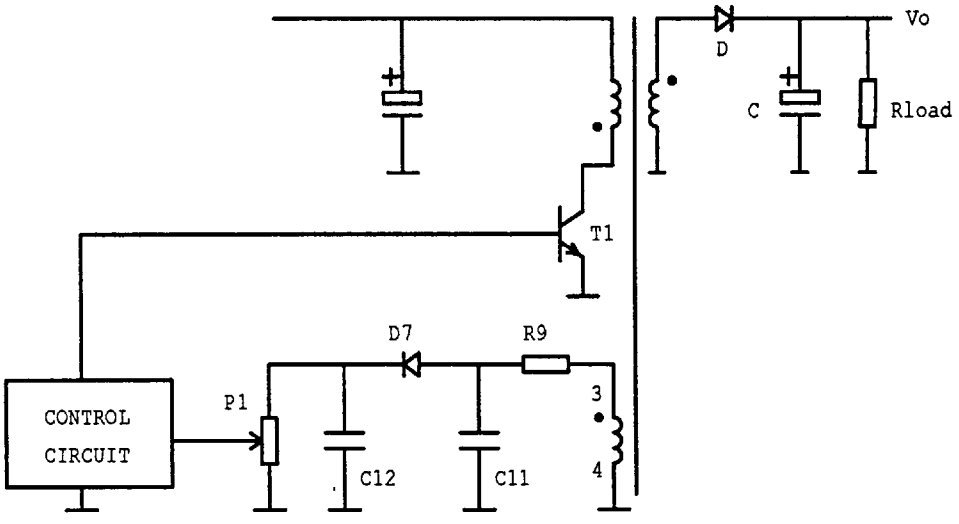

Figure 2. Basic circuit diagram

The control IC TDA8380 directly drives the power output transistor. When the transistor conducts, a linearly increasing current flows through the primary winding of the transformer. As a consequence energy is stored in the transformer. After switching off the transistor, the stored energy is transferred into the load via diode D. During the time that the transistor is not conducting, the flyback voltage at the control winding (3-4) is rectified via diode D7, smoothed by C12 and divided by R10, R13 and P1 (chapter 9). The parasitic swing, which is due to the ringing of the transformer, is filtered by R9 and C11. By controlling the duty cycle of the drive pulses, the output voltage Vo is kept constant.

The flyback converter under discussion has been designed for the interrupting current mode. The principle of this circuit has already been described in several PCALE and PCALM reports a.o. in reference [1]. For a nominal output voltage of 115V, Vmainsmin=90Vrms and a fixed frequency of 26kHz, the maximum load is 55W.

3. CIRCUIT DIAGRAM.

The circuit diagram is given in chapter 9. In this chapter detailed information is given about several parts of the supply.

3.1 Mains input part.

Diodes D1 to D4 rectify the mains input voltage and the DC supply to the SMPS is smoothed by C8. If C8 is fully discharged, the inrush current has to be limited by R1 to protect the rectifier diodes. The RFI filter consists of C1, L1 and C2. Capacitors C4 to C7 suppress the RFI generated by the diodes in the mains bridge rectifier. The degaussing circuit consists of C3 and PTC R38.

3.2 Start-up supply.

The control IC TDA8380 receives its start-up supply from the mains rectified voltage by the low wattage resistor R2. During the time leading up to the initialization of the IC, base coupling capacitor C19 is pre-charged. So the power switching transistor T1 is switched off correctly during the start-up period. The IC is initialised as soon as the voltage on the supply pin 5 reaches 17V. This takes approximately 1 sec. at Vmains= 220Vrms. Shorter times are possible by lowering the value of R2 or choosing an alternative start-up circuit. Now the SMPS will start up and the duty cycle will be slowly increased by the slow-start circuit. The take-over supply is derived via diode D6 from the flyback auxiliary winding (3-4) on the transformer (AT3010/110LL).

3.3 Control IC.

The integrated SMPS control circuit TDA8380 offers many attractive operating facilities. It controls the SMPS power throughput and regulation by pulse-width modulation. The IC can directly drive the power switching transistor and it can operate free-running or line locked.
A detailed description is given in Reference [2].
The function of each pin is described below.

Pin 1 Emitter of the forward drive transistor. It directly drives the power transistor with a source current of about 0.4A (max. 0.75A).

Pin 2 Collector of the forward transistor. This pin is connected via R6 to the IC supply. Resistor R6 and R21 mainly determine the source current of the power switching transistor.

Pin 3 Demagnetization sensing. For this flyback converter, operating in the discontinuous current mode, the voltage across the SMPS transformer is sensed via R5 and R7.

Pin 4 Low supply-voltage protection level. This pin is connected to ground, so the Vccmin of the IC is set at 8.4V.

Pin 5 IC supply. When the mains input is applied to the SMPS, the IC supply reservoir capacitor C10 is charged by a current determined by resistor R2. When the voltage at pin 5 reaches 17V, the IC initializes and diode D6 rectifies the flyback signal from winding 3-4 of the SMPS transformer to supply the IC with 18V.

Pin 6 Master reference current setting. Resistor R8 sets the master reference current for the TDA8380 to 500 μA.

Pin 7 Error amplifier input and undervoltage (open loop) protection (TCG). The internal reference voltage is 2.5V .

Pin 8 Output of the error amplifier. This is the error amplifier output pin that allows the connection of external frequency compensation network C13/R14.

Pin 9 Duty. This is the input of the pulse-width modulator and it is normally connected to pin 8.

Pin 10 Oscillator. A 750pF capacitor C16 is connected to this pin; together with resistor R8 (5K1) the oscillator frequency is set to 26kHz.

Pin 11 Synchronization. Not used.

Pin 12 Slow-start (capacitor C17) and maximum duty cycle (R19).

Pin 13 Overcurrent protection. The overcurrent protection safeguards the power switching transistor for being overloaded with a too high collector peak current.

Pin 14 Ground.

Pin 15 Emitter of the reverse drive transistor, connected to ground.

Pin 16 Collector of the reverse drive transistor.

3.4 SMPS transformer.

The SMPS transformer (AT3010/110LL) provides mains isolation. It is an aluminium foil transformer of which the magnetic circuit comprises two Ferroxcube ETD-cores with a rectangular leg and a cylindrical leg on which the windings are situated. The transformer contains one internal screen which is, for EMC reasons, connected to the DC supply.
At Vmains=90Vrms the output power is restricted to 55W. A higher output power is possible by reducing the frequency (R8,C16) or restricting the mains voltage range.
The energy stored in the leakage inductance will be dissipated in the dV/dt limiter (D5,C9,R3) and the energy stored in the parasitic winding capacitances in the power switching transistor T1 and the damping network (C25,R28).

3.5 Power switching transistor.

At an output power of 55W, the Icmax of the power switching transistor BUT11A is approx. 1.9A. The forward base drive is determined by the supply voltage of the IC, zener voltage D10 and resistors R6 and R21. The negative base drive is provided by capacitor C19, which acts as a voltage source equal to the zener voltage D10. During the turn off, the sink transistor of the TDA8380 is conducting. This means that a negative base current with a -dI/dt, which is determined by the zener voltage D10 and L2, switches off transistor T1. The diode D9 ensures that the negative voltage at pin 1 of the TDA8380 is restricted. The dV/dt limiter consists of C9, D5 and R3. R22 in combination with C20 damps the ringing of the base-emitter and prevents parasitic switch-on of T1 during the flyback. Resistor R23 ensures that transistor T1 remains switched off during the initialisation phase of the IC.

On pages 21 and 22 the circuit diagrams are given of 2 Switched Mode Power Supplies, euipped with a Power MOSFET.

3.6 Secondary rectifiers.

The three secondary flyback rectifiers deliver: 115V (line deflection supply), 26V (vertical deflection and/or sound supply) and 16V (small signal supply). The load determines the dissipation in the diodes and also the value of the electrolytic capacitors. It is also possible, by choosing another tap on the transformer, to obtain 145V, 105V, 25V or 8V.
To prevent interference between the SMPS switching frequency and the line deflection frequency, an L-C filter has been added in the 115V supply. The inductor is L6 (AT4043/11) while the capacitor is located on the line deflection board.

3.7 Error-amplifier.

The flyback voltage from winding 3-4 of the SMPS transformer is smoothed by R9/D7/C12, to give a DC level that varies in proportion to variations of the output from the SMPS. This level is reduced by the divider R10/R13/P1 and fed to error-amplifier (pin 7) of the TDA8380. The signal which is fed to this pin, is compared with an internal reference voltage. C13/R14 is the external frequency compensation network. Below $f1=1/2\pi R14C13$, the circuit behaves like an integrator, giving a high DC stabilization and ripple rejection.
Before the output signal of the error-amplifier is fed to the pulse-width modulator, it is filtered by R17 and C15, giving a high frequency roll-off above $f2 (=1/2\pi R17C15)$.
The SMPS output level is set by P1.

3.8 Standby.

During the standby mode the small signal supply of the TV is switched off by transistors T3 to T5. As a result the line oscillator stops, the deflection disappears and the sound and video output stages are no longer driven.
If no measures were taken, the output voltages would increase to an unacceptable high level (120%). However at the same time the feedback is modified, through which VC12 reduces to 85%. As a result the output voltages will be reduced to 95-100%. (see osc. 6, page 20)
The loopstability of the SMPS in the standby mode can be improved by reducing the openloop gain. This is achieved by switching the feedback of the error amplifier (see page 14). For this reason resistors R39, R40, R41 and diode D15 are added.
The appropriate Bode plot is given in osc. 5 page 20; measurement condition: Vmains = 220Vrms and 110Vrms at Po=55W.
During the standby mode the SMPS still operates in the fixed frequency mode and the input power at the mains is 7W. Pre-load R29 (0.5W) ensures correct operation of the SMPS when there is no external load. It can be removed in an actual TV set.
The modification of the feedback in the standby mode is achieved in the following way: if the load reduces, the pulsewidth of the flyback pulse decreases. If the pulsewidth reduces below a certain minimum level, transistor T2 is switched off and herewith the feedback is increased.